Hi3516D Professional HD IP Camera SoC

# Brief Data Sheet

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# Hi3516D Professional HD IP Camera SoC

# Key Specifications

## Processor Core

- A7@600 MHz, 32 KB I-cache, 32 KB D-cache/128 KB L2 cache
- Neon acceleration, integrated FPU

## Video Encoding

- H.264 BP/MP/HP
- H.265 main profile
- MJPEG/JPEG baseline encoding

## Video Encoding Performance

- A maximum of 5-megapixel resolution for H.264/H.265 encoding
- Real-time H.264/H.265 encoding of multiple streams:
  - 1080p@30 fps+720p@30 fps+VGA@30 fps
  - 3-megapixel@30 fps+VGA@30 fps
  - 5-megapixel@15 fps
- JPEG snapshot at 5-megapixel@8 fps
- Supporting the CBR/VBR bit rate control mode, ranging from 16 kbit/s to 40 Mbit/s
- Encoding frame rate ranging from 1/16 fps to 240 fps
- Encoding of eight ROIs

## Intelligent Video Analysis

- Integrated IVE, supporting various intelligent analysis applications such as motion detection, boundary security and video diagnosis

## Video and Graphics Processing

- 3D denoising, image enhancement, and dynamic contrast enhancement
- Anti-flicker for output videos and graphics
- 1/15.99x to 16x video scaling
- 1/2x to 2x graphics scaling
- OSD overlay pre-processing for eight regions
- Video graphics overlaying of two layers (video layer and graphics layer)

## ISP

- Adjustable 3A functions (AE, AWB, and AF)
- Noise reduction in FPN mode
- Highlight compensation, backlight compensation, gamma correction, and color enhancement
- Defect pixel correction, denoising, and digital image stabilizer
- Anti-fog
- Lens distortion correction
- Picture rotation by 90° or 270°
- Mirroring and flipping
- Digital WDR, frame base/line base WDR, and tone mapping

- ISP tuning tools for the PC

## Audio Encoding/Decoding

- Voice encoding/decoding in compliance with multiple protocols by using software
- G.711, ADPCM, and G.726 protocols
- AEC, ANR, and ALC

## Security Engine

- Various encryption and decryption algorithms using hardware, such as AES, DES, and 3DES
- Digital watermark

## Video Interfaces

- Input
  - 8-/10-/12-/14-bit RGB Bayer DC timing VI, a maximum of 150 MHz clock frequency
  - BT.601, BT.656 or BT.1120 VI interface
  - MIPI, LVDS/sub-LVDS, and HiSPI
  - Compatibility with mainstream HD CMOS sensors provided by Sony, Aptina, OmniVision, and Panasonic
  - Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
  - Programmable sensor clock output
  - Maximum input resolution of 5 megapixels
- Output
  - One PAL/NTSC output for automatic load detection
  - One BT.1120/BT.656 VO interface for connecting to an external HDMI or SDI, up to 1080p@60 fps output

## Audio Interfaces

- Integrated audio CODEC, supporting 16-bit audio inputs and outputs
- $I^2S$ interface for connecting to an external audio CODEC

## Peripheral Interfaces

- POR
- One integrated high-precision RTC
- One dual-channel SAR ADC
- Four UART interfaces
- One IR interface, three $I^2C$ interfaces, four SPI master interfaces, 14 x 8 + 3 GPIO interfaces
- Eight PWM interfaces (four independent interfaces and four multiplexed with other pins)
- Two SDIO 3.0 interfaces, supporting SDXC
- One USB 2.0 host/device port
- RGMII/RMII/MII in 100/1000 Mbit/s full-duplex or half-duplex mode, PHY clock output, and TSO network acceleration

## External Memory Interfaces

- DDR3/3L SDRAM interface
  - One 16-bit DDR3/3L interface with the maximum frequency of 600 MHz (1.2 Gbit/s)
  - Maximum capacity of 4 Gbits for a 16-bit DDR

- SPI NOR flash interface
  - 1-, 2-, or 4-wire mode
  - Maximum capacity of 32 MB
- SPI NAND flash interface
  - Maximum capacity of 4 Gbits
- NAND flash interface
  - 8-bit data width
  - SLC or MLC
  - 4-, 8-, or 24-bit ECC
  - Components with 8 GB capacity or larger
- Booting from the SPI NOR flash, SPI Nand Flash or NAND flash

## SDK

- Linux-3.4-based SDK
- High-performance H.264/H.265 PC decoding library

## Physical Specifications

- Power consumption
  - 900 mW typical power consumption
  - Multi-level power-saving mode
- Operating voltages
  - 1.1 V core voltage
  - 3.3 V I/O voltage and 3.8 V margin voltage
  - 1.35 V or 1.5 V DDR3/3L SDRAM interface voltage
- Package
  - Body size of 15 mm x 15 mm (0.59 in. x 0.59 in.), 0.65 mm (0.03 in.) ball pitch, TFBGA RoHS

# Functional Block Diagram
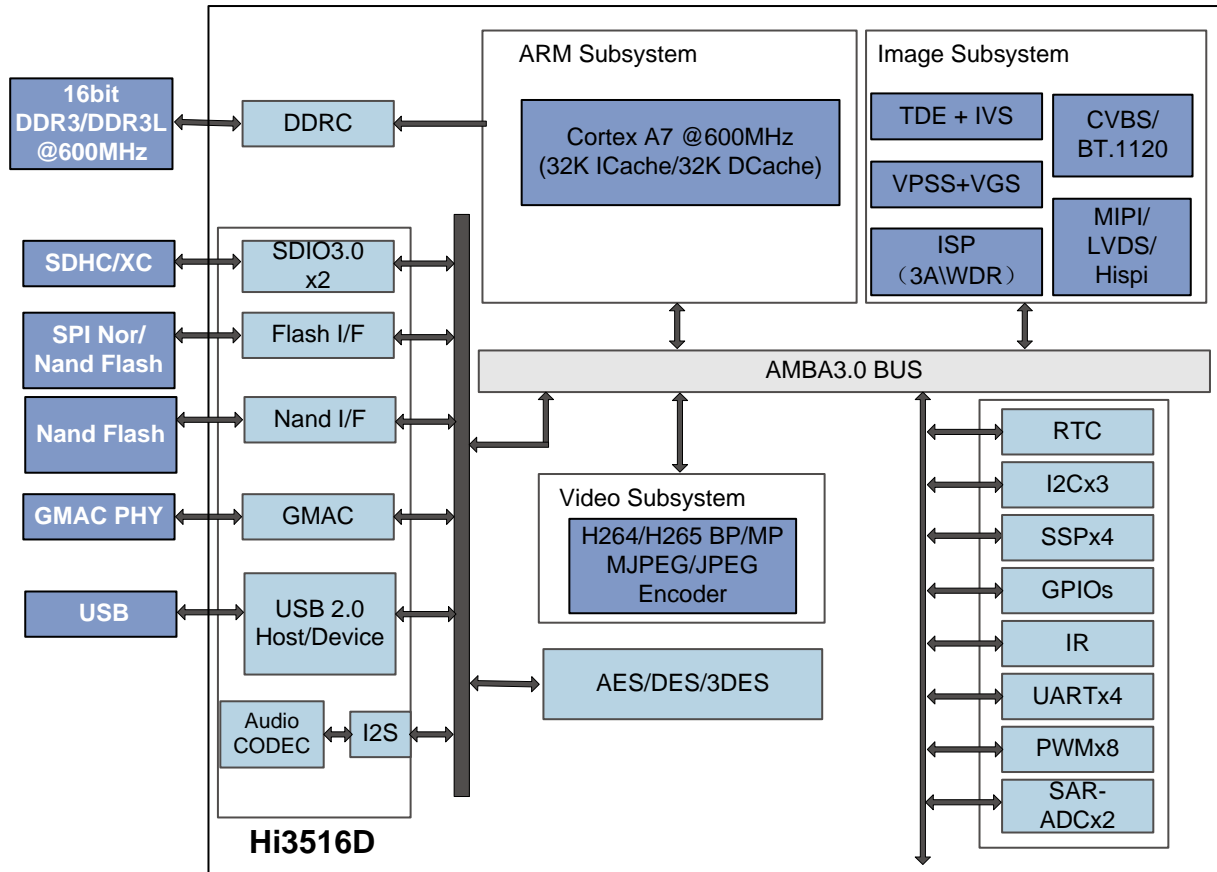


As a new-generation SoC designed for the HD IP camera, the Hi3516D integrates a new-generation ISP and adopts the latest H.265 compressed video encoder, advanced low-power technology, and low-power architecture design. These features help the Hi3516D keep the leading position in the aspects of low bit rate, high picture quality, and low power consumption. The Hi3516D supports 90° or 270° rotation and lens distortion correction, which meets requirements in various surveillance applications. It also fully supports 3A algorithms, which allow customers to design different types of IP cameras including the IP AF zoom module. The Hi3516D integrates the POR, RTC, and audio CODEC and supports various sensor levels and clock outputs, which significantly reduces the EBOM costs for the Hi3516D HD IP camera. Similar to other HiSilicon DVR and NVR SDKs, the Hi3516D SDK features high stability and ease of use, which allows rapid mass production and facilitates system layout of IP cameras, DVRs, and NVRs.

**Hi3516D Professional HD IP Camera SoC**

# Hi3516D HD IP Camera Solution
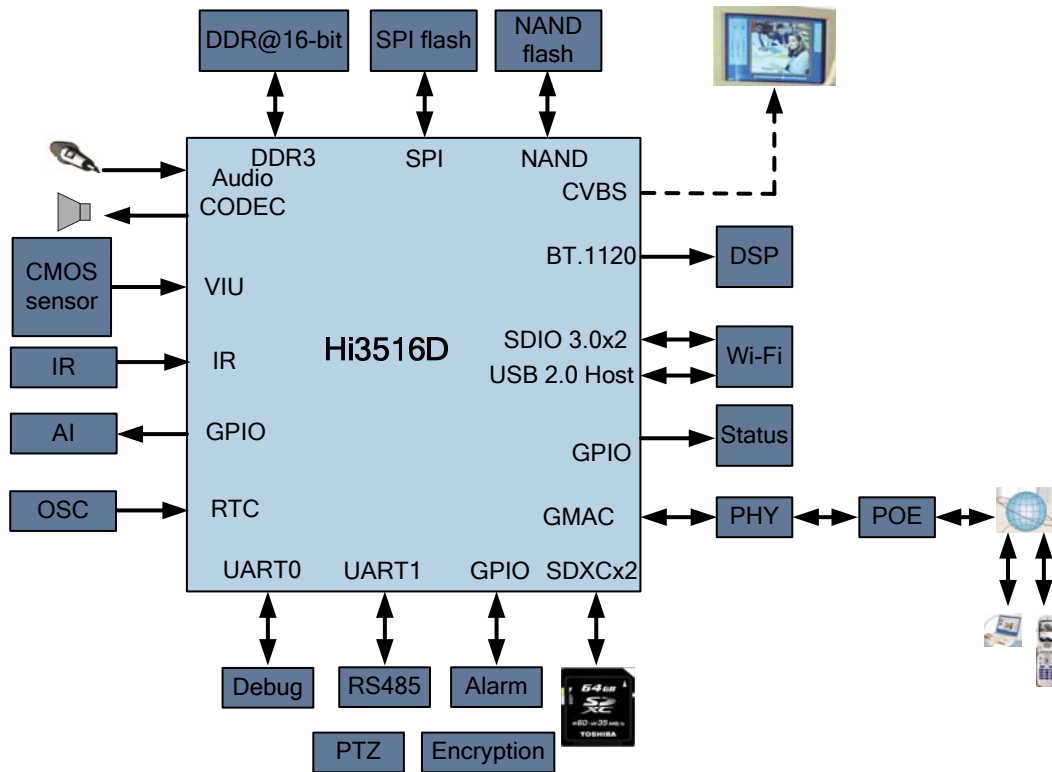


# Acronyms and Abbreviations

| | |
|---|---|
| 3DES | triple data encryption standard |
| ABR | average bit rate |
| ADC | analog-to-digital converter |
| AE | automatic exposure |
| AEC | acoustic echo cancellation |
| AES | advanced encryption standard |
| AF | automatic focus |
| ALC | auto level control |
| ANR | audio noise reduction |
| AWB | automatic white balance |
| CBR | constant bit rate |
| CMOS | complementary metal-oxide semiconductor |
| CODEC | coder/decoder |
| DES | data encryption standard |
| DVR | digital video recorder |
| ECC | error correcting code |
| FPN | fixed pattern noise |
| FPU | floating point unit |
| GPIO | general-purpose input/output |
| HD | high definition |
| HDMI | high-definition multimedia interface |
| $I^2C$ | inter-integrated circuit |

| | |
|---|---|
| I²S | inter-IC sound |
| IR | infrared |
| ISP | image signal processor |
| LVDS | low-voltage differential signaling |
| IVE | intelligent video engine |
| MIPI | mobile industry processor interface |
| MLC | multi-level cell |
| NTSC | National Television Systems Committee |
| NVR | network video recorder |
| OSD | on-screen display |
| PAL | phase alternating line |
| PHY | physical |
| POR | power-on-reset |
| PWM | pulse width modulation |
| RGMII | reduced gigabit media independent interface |
| RMII | reduced media independent interface |
| RoHS | Restrictions on the Use of Certain Hazardous Substances |
| ROI | region of interest |
| RTC | real-time clock |
| SAR | successive approximation |
| SDI | serial digital interface |
| SDIO | secure digital input/output |
| SDK | software development kit |
| SDRAM | synchronous dynamic random access memory |
| SDXC | secure digital extended capacity |
| SLC | single-level cell |
| SoC | system-on-chip |
| SPI | serial peripheral interface |
| TFBGA | thin & fine-pitch ball grid array |
| TSO | TCP segmentation offload |
| UART | universal asynchronous receiver transmitter |
| VBR | variable bit rate |
| VI | video input |
| VO | video output |
| WDR | wide dynamic range |